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Fitzgerald, Eugene, JR.

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14. ABSTRACT

In this program, we have been able to advance materials and device work in the area of lattice-mismatched semiconductor materials. In the silicon-germanium materials system, we have explored the use of strained layers to getter hydrogen implanted into the layers for an exfoliation process. This layer transfer technique was used to demonstrate germanium on insulator (GOI) substrate formation using virtual Ge/Si wafers. In III-V materials systems, we have investigated the formation of cracks during GaAs growth on virtual Ge/Si Substrates, defining critical thickness for crack formation. We also compare luminescence efficiency in InGaAs quantum wells on GaAs/Si, GaAs/Ge/SiGe/Si, GaAs and GaAs/Ge, and show that the integrated intensity of the InGaAs QW on GaAs/Ge/SiGe/Si and GaAs are nearly equivalent. We have demonstrated continuous-wave room temperature lasing of GaAs lasers on silicon.

15. SUBJECT TERMS

lattice mismatched, semiconductors, integrated optoelectronics, engineered substrates, germanium on insulator

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1. List of Papers Submitted or Published, Presentations

Publications/Presentations with ARO support (appeared or submitted in 7/03 – 1/05)

(a) Manuscripts submitted, but not published:

O. Kwon, M.L. Lee, A.J. Pitera, E.A. Fitgzerald and S.A. Ringel, "*Room temperature operation of AlGaInP laser diodes grown on metamorphic SiGe/Si substrate by solid source molecular beam epiatxy*," submitted, J. Appl. Phys. (2005).

M. Lueck, C.L. Andre, A.J. Pitera, M.L. Lee, E.A. Fitzgerald and S.A. Ringel, "*Dual Junction InGaP/GaAs Solar Cells Grown on Metamorphic SiGe Substrates*," accepted pending minor revision, IEEE Electron Devices Letters (2005).

(b) Manuscripts published in peer-reviewed journals:

Arthur J. Pitera and E. A. Fitzgerald, "Hydrogen gettering and strain-induced platelet nucleation in tensilely strained $Si_{0.4}Ge_{0.6}$/Ge for layer exfoliation applications", Journal of Applied Physics **97**, 104511 (2005). [993 K, 11 pages]

N. Ariel, G. Ceder, D. Sadoway, E. A. Fitzgerald, "*Electrochemically controlled transport of lithium through ultrathin SiO_2*", Journal of Applied Physics **98**, 023516 (2005). [351 K, 7 pages]

C.L. Andre, D.M. Wilt, A.J. Pitera, M.L. Lee, E.A. Fitzgerald and S.A. Ringel, "*Comparative Impact of Dislocation Densities on n+p and p+n Junction GaAs Diodes and Solar Cells on SiGe Virtual Substrates,"* J. Appl. Phys. 98, pp. 014502: 1-5(2005).

O. Kwon, Y. Lin, J.J. Boeckl and S.A. Ringel, "*Properties of digitally-alloyed AlGaInP grown by solid source molecular beam epitaxy*," J. Electron. Mater. 34, pp. 1-6 (2005).

C.L. Andre, J.A. Carlin, J.J. Boeckl, D.M. Wilt, M.A. Smith, A.J. Pitera, M.L. Lee, E.A. Fitzgerald, and S.A. Ringel, "*Investigations of high performance GaAs solar cells grown on Ge-SiGe-Si substrates*," IEEE Trans. El. Dev. 52, pp. 1055-1060 (2005)

M.K. Hudait, Y. Lin, S.H. Goss, P. Smith, S. Bradley, L.J. Brillson, S.W. Johnston, R.K. Ahrenkiel and S.A. Ringel, ""*Evidence of interface-induced persistent photoconductivity in InP/In0.53Ga0.47As/InP double heterostructures grown by molecular beam epitaxy*," Appl. Phys. Lett. 87, pp. 032106: 1-3 (2005).

Y. Lin, M.K. Hudait, S.W. Johnston, R.K. Ahrenkiel and S.A. Ringel, "*Photoconductivity Decay Study of Metamorphic InAsP/InGaAs Heterostructures Grown by Molecular Beam Epitaxy*," Appl. Phys. Lett. 86, pp. 071908: 1-3 (2005).

O. Kwon, J.J. Boeckl, M.L. Lee, A.J. Pitera, E.A. Fitzgerald and S.A. Ringel, "*Growth and Properties of AlGaInP Resonant Cavity Light E*mitting Diodes on Ge/SiGe/Si Substrates*," J. Appl. Phys. 97, pp. 1-6 (2005).

P.E. Smith, S.H. Goss, S.T. Bradley, M.K. Hudait, Y. Lin and S.A. Ringel, "Atomic Layer Diffusion and Electronic Structure at $In_{0.53}Ga_{0.47}As$/InP Interfaces," Appl. Phys. Lett. J. Vac. Sci. and Technol. B 22, pp. 554-559 (2004).

M.K. Hudait, Y. Lin, M.N. Palmisiano, C. Tivarus, J.P. Pelz and S.A. Ringel, "*Comparison of mixed anion InAsP and mixed cation InAlAs metamorphic buffers grown by molecular beam epitaxy on (100) InP substrates*," J. Appl. Phys. 95, pp. 3952-3960 (2004).

L. M. McGill, E. A. Fitzgerald, A. Y. Kim, J.-W. Huang, S. S. Yi, P. N. Grillot, and S. A. Stockman, "*Microstructural Defects in Metalorganic Vapor Phase Epitaxy of Relaxed, Graded InGaP: Branch Defect Origins and Engineering"* J. Vac. Sci. Technol. B, Vol. 22 (4) p.1899 (2004)

D. M. Isaacson, G. Taraschi, A. Pitera, N. Ariel, T. A. Langdo, and E. A. Fitzgerald, *"Strained silicon on silicon by wafer bonding and layer transfer from relaxed SiGe buffer"*, ECS Meeting Proceedings (2004).

A. J. Pitera, G. Taraschi, M. L. Lee, C. W. Leitz, Z.Y. Cheng, and E. A. Fitzgerald "*Coplanar integration of lattice-mismatched semiconductors with silicon by wafer bonding Ge/$Si_{1-x}Ge_x$/Si virtual substrates", J*ournal of the Electrochemical Society **151** (7), G443 (2004). [664 K, 5 pages]

C.L. Andre, J.J. Boeckl, D.M. Wilt, A.J. Pitera, M.L. Lee, E.A. Fitzgerald, B.M. Keyes and S.A. Ringel, "*Impact of dislocations on minority carrier electron and hole lifetimes in GaAs grown on metamorphic SiGe substrates*," Appl. Phys. Lett. 84, pp. 3447-3449 (2004).

O. Kwon, Y. Lin, J. Boeckl and S.A. Ringel, "*Growth and Properties of Digital Alloyed AlGaInP by Solid Source Molecular Beam Epitaxy*," submitted to Journal of Electronic Materials, (2003)

Andre, C.L., J. J. Boeckl, C.W. Leitz, M.T. Currie, T. A. Langdo, E.A. Fitzgerald and S.A. Ringel, "*Low Temperature GaAs Films Grown on Ge and Ge/SiGe/Si Substrates*" Journal of Applied Physics, **94** (8) p. 4980 (2003)

O. Kwon, M.M. Jazwiecki, R.N. Sacks and S.A. Ringel, " High performance, metamorphic InGaAs tunnel diodes grown by molecular beam epitaxy," IEEE Electron Dev. Lett. 24, pp. 613-615 (2003).

M.K. Hudait, Y. Lin, M.N. Palmisiano and S.A. Ringel, "*0.6 eV bandgap $In_{0.69}Ga_{0.31}As$ thermophotovoltaic devices grown on InAsP ste-graded buffers by molecular beam epitaxy*," IEEE Electron Dev. Lett. 24, pp. 538-540 (2003).

M.K. Hudait, Y. Lin, D.M. Wilt, F. Wu, J.S. Speck, C.A. Tivarus, E.R. Heller, J.P. Pelz and S.A. Ringel, "*High-quality InAsP step-graded buffer by molecular beam epitaxy*," Appl. Phys. Lett. Vol. 82, pp. 3212-3214 (2003).

Groenert, M.E., C.W. Leitz, A.J. Pitera, V.K. Yang, H. Lee, R.J. Ram, and E.A. Fitzgerald, *"Monolithic integration of room-temperature cw GaAs/AlGaAs lasers on Si substrates via relaxed graded GeSi buffer layers"* Journal of Applied Physics, **93** (1) p. 362-367 (2003)

Groenert, M.E., A.J. Pitera, Rajeev J. Ram, and E.A. Fitzgerald, *"Improved room-temperature cw GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers fabricated on Si substrates via relaxed graded $GexSi_{(1-x)}$ buffer layers"*, Journal of Vacuum Science and Technology, B21, p.1064 (2003)

Yang, V.K., M. Groenert, C.W. Leitz, A. J. Pitera, M.T. Currie, and E. A. Fitzgerald, *"Crack Formation in GaAs heteroepitaxial films on Si and SiGe virtual Substrates"*, Journal of Applied Physics, **93** (7) p. 3859-3865 (2003)

Yang, V.K., S.M. Ting, M.E. Groenert, M.T. Bulsara, M.T. Currie, C.W. Leitz, and E.A. Fitzgerald, *"Comparison of Lumisnescent Efficiency of InGaAs Quantum Well Structures Grown on Si, GaAs, Ge, and SiGe Virtual Substrate"*, Journal of Applied Physics, **93** (9) p. 5095-5102, (2003)

S.A. Ringel, J.A. Carlin, C.L. Andre, M.K. Hudait, M. Gonzalez, D.M. Wilt, E.B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E.A. Fitzgerald and C.W. Leitz, "*Single junction InGaP/GaAs Solar Cells*

Grown on Si Substrates with SiGe Buffer Layers," (**Invited**) Progress in Photovoltaics: Research and Applications Vol. 10, pp. 417-426 (2002).

J.A. Carlin, S.A. Ringel, E.A. Fitzgerald and M. Bulsara, "*High lifetime GaAs on Si using GeSi buffers and its potential for space applications,"* Solar Energy Materials and Solar Cells vol. 66, pp. 621-630, 2001.

(c) Papers published in non-peer-reviewed journals or in conference proceedings:

McGill, L.M., J. Wu and E. A. Fitzgerald, *"Yellow-Green emission for ETS-LEDs and lasers based on a strained InGaP quantum well heterostructure grown on a transparent, compositionally graded AlInGaP buffer"*, Mat. Res. Soc. Symp. Proc., Vol. 744 (2003).

O.Kwon, J.J. Boeckl, M.L. Lee, A. Pitera, E.A. Fitzgerald and S.A. Ringel, "Growth and Properties of AlGaInP Resonant Cavity Light Emitting Diodes (RCLEDs) on Ge/SiGe/Si Substrates", Mater. Res. Soc. Symp. (Boston, MA) Proc. In Print (2003)

S.A. Ringel and C.L. Andre, D. M. Wilt, E.A. Fitzgerald, M.Lee, A. Pitera, M.Smith, D. Scheiman and P. Jenkins, *"Advances in p+n and n+p GaAs Solar Cells Grown on SiGe/Si Substrates"*, 18th Space Photovoltaic Research and Technology Conference (Cleveland, OH) (2003)

(d) Papers presented at meetings but not published in conference proceedings: None

Conference Papers and Presentations (past year)

S.A. Ringel, "*Defect Engineering in III-V/Si Integration and Applications for Optoelectronics and Photovoltaics*," (Invited), ICMAT (Singapore) 2005

O. Kwon,A. J. Pitera, M. L. Lee, E. A. Fitzgerald, and S. A. Ringel, "*Room temperature operation of AlGaInP laser diodes monolithically integrated on metamorphic SiGe/Si substrates*," ICMAT (Singapore) 2005

M. Gonzalez, C. L. Andre, R.J. Walters, S.R. Messenger, J.H. Warner, J.R. Lorentzen, David M. Wilt, E.A. Fitzgerald and Steven A. Ringel, "R*adiation Study of GaAs Solar Cells Grown on SiGe Substrates*," Proc. European Photovoltaic Solar Energy Conference and Exhibition (in print), Barcelona (2005).

M. Gonzalez, C. L. Andre, R.J. Walters, S.R. Messenger, J.H. Warner, J.R. Lorentzen, David M. Wilt, E.A. Fitzgerald and Steven A. Ringel, "*Deep Level Defects in GaAs Grown on Metamorphic SiGe Substrates and Evidence for Dislocation-Enhanced Point Defect Gettering,*" 47th IEEE/TMS Electronic Mater. Conf. (Santa Barbara, CA), 2005.

C. Tivarus, J.P. Pelz, M. K. Hudait, and S.A. Ringel, "*Nanoscale Characterization of Metal/Semiconductor Nanocontacts and Nano-structured Metal/Insulator Interfaces*," International Conference on Characterization and Metrology for ULSI Technology, March 15-18 (2005), The University of Texas at Dallas, Richardson, Texas, USA.

S.A. Ringel, C.L. Andre, E.A. Fitzgerald, A.J. Pitera and D.M. Wilt, *"Multi-Junction III-V Photovoltaics on Lattice-Engineered Si Substrates*," Proc. IEEE Photovoltaic Specialists Conf., Orlando, (2005).

Matthew Lueck, María González, Ojin Kwon, Carrie Andre, and Steven A. Ringel, "*Impact of Annealing and III:V ratio on properties of MBE-grown wide bandgap AlGaInP materials and solar cells*," Proc. IEEE Photovoltaic Specialists Conf., Orlando, (2005).

D.M. Wilt, A.T. Pal, N.R. Prokop, S.A. Ringel, C.L. Andre, M.A. Smith, D.A. Scheiman, P.P. Jenkins, W.F. Maurer, B. McElroy and E.A. Fitzgerald, *"Thermal Cycle Testing of GaAs o SI and Metamorphic Tandem on Si Solar Cells*," Proc. IEEE Photovoltaic Specialists Conf. (Orlando), in print (2005).

S.A. Ringel, C.L.Andre, M. Lueck, D. Isaacson, A.J. Pitera, E.A. Fitzgerald and D.M. Wilt, "*III-V Multi-Junction Materials and Solar Cells on Engineered SiGe/Si Substrates*," (**Invited**) Mater. Res. Soc. Symp. (Boston, MA), Proc. in print (2005).

C. Tivarus, J.P. Pelz, M.K. Hudait and S.A. Ringel, "*Cross-Sectional Ballistic Electron Emission Microscopy Studies of Molecular Beam Epitaxy Grown Quantum Wells*," 51st Meeting of the American Vacuum Society (Anaheim, CA), 2004.

M.K. Hudait, Y. Lin and S.A. Ringel, "*Strain Relaxation of Ste-Graded Metamorphic InAsP Buffers on InP Substrates*," 51st Meeting of the American Vacuum Society (Anaheim, CA), 2004.

M. Gonzalez, C.L. Andre, R.J. Walters, S.R. Messenger, J.H. Warner, J.R. Lorentzen, D.M. Wilt, M. Smith, A.J. Pitera, M.L. Smith, E.A. Fitzgerald and S.A.Ringel, "*Grown-In and Radiation-Induced Defects in High Performance GaAs Solar Cells on SiGe/Si,"* Proc. 19th European Photovoltaic Solar Energy Conversion Conf. (Paris), pp. 3735-3738 (2004).

D.M. Wilt, S.A.Ringel, C.L. Andre, M.A. Smith, D.A. Scheiman, P.P. Jenkins, E.A. Fitzgerald, R.J. Walters, S.R. Messenger, J.H. Warner, J.R. Lorentzen, W.F. Maurer and E.B.Clark, "*LEO Testing of GaAs on Si Solar Cells Aboard MISSE5*," Proc. 19th European Photovoltaic Solar Energy Conversion Conf. (Paris), pp. 3602-3605 (2004).

M.K. Hudait, Y. Lin and S.A. Ringel, "*Comparison of Mixed Anion InAsP and Mixed Cation InAlAs Metamorphic Buffers Grown by MBE on InP Substrates and Device Implications*," 46th IEEE/TMS Electronic Mater. Conf. (South Bend, IN), 2004.

O. Kwon, J. J. Boeckl, M.L. Lee,A. Pitera, E.A. Fitzgerald and S.A. Ringel, *"High Performance AlGaInP Resonant Cavity Light Emitting Diodes (RCLEDs) on relaxed SiGe/Si Substrates*," SPIE Great Lakes Photonics Symposium (2004).

O.Kwon, J. J. Boeckl, M.L. Lee, A. Pitera, E.A. Fitzgerald and S.A. Ringel, "*Growth and Properties of AlGaInP Resonant Cavity Light Emitting Diodes (RCLEDs) on Ge/SiGe/Si Substrates*," Mater. Res. Soc. Symp. (Boston, MA) Proc. Vol. 799, pp. Z3.4.1 – Z3.4.6 (2004).

S.A. Ringel and C.L. Andre, D.M. Wilt, E.A. Fitzgerald, M. Lee, A. Pitera, M. Smith, D. Scheiman and P. Jenkins, "*Advances in p^+n and n^+p GaAs solar cells grown on SiGe/Si substrates*," 18th Space Photovoltaic Research and Technology Conf. (Cleveland), 2003.

Fitzgerald, E.A., M.L. Lee, C.W. Leitz and D.A. Antoniadis, "*MOSFET Channel Engineering Using Strained Si, SiGe, and Ge Channels*", **(Invited)**, 203rd Electrochemical Society Meeting, Spring, April 27-May 2nd 2003, Volume 2003-01, (Paris, France) 2003

Fitzgerald, E.A., "*SiGe MOSFET Heterostructures*" **(Invited)**, Annual APS Meeting, March 3-7, (Austin, TX) 2003

Fitzgerald, E.A., M.L. Lee, C.W. Leitz, and D.A. Antoniadis, *"Strained Si, SiGe, and Ge MOSFET Channels"*, **(Invited)**, ICS13, Third International Conference on SiGe (C) Epitaxy and Heterostructures, March 9-12th, (Santa Fe, New Mexico) 2003

S.A. Ringel, C. Andre, M. Gonzalez, M. Hudait, D. Wilt, E. Clark, A. Pitera, M. Lee, E. Fitzgerald, M. Carroll, M. Erdtmann, J. Carlin and B. Keyes, "*Toward High Performance n/p GaAs Solar Cells Grown on Low Dislocation Density p-type SiGe Substrates*," 30th IEEE Photovolt. Spec. Conf. and 3rd World Conf. On Photovoltaic Energy Conversion (WCPEC-3), May 12-16 (Osaka, Japan) 2003

Pitera, A. J., G. Taraschi, M.L. Lee, C.W. Leitz, Z.Cheng, and E.A. Fitzgerald, *"CMOS-Compatible Platform for Ge and III-V Integration with Si"*, ICS13, Third International Conference on SiGe (C) Epitaxy and Heterostructures, March 9-12th, (Santa Fe, New Mexico) 2003

C.L. Andre, M. Gonzalez, D.M. Wilt, E.B. Clark, A.J. Pitera, M.L. Lee, E.A. Fitzgerald, M. Carroll, M. Erdtmann, J.A. Carlin, B.M. Keys and S.A. Ringel, "*Correlation of minority carrier electron and hole lifetimes and the reverse saturation current density in GaAs diodes grown on Ge/SiGe/Si substrates*," 45th TMS Electronic Materials Conference, June 23-27th (Salt Lake City, UT) 2003

Fitzgerald, E.A., *"The Science and Applications of Relaxed Semiconductor Alloys on Conventional Substrates"*, **(Invited)**, 3rd World Conference on Photovoltaic Energy Conversion, May 12-16th, (Osaka International Convention Center, Osaka, Japan) 2003

O. Kwon, J. J. Boeckl, M.L. Lee, A. Pitera, E.A. Fitzgerald, and S.A. Ringel, "*Monolithic Integration of AlGaInP Light Emitting Diodes on Si Substrates,"* 45th TMS Electronic Materials Conference, June 23-27th (Salt Lake City, UT) 2003

Fitzgerald, E.A., *"Strained Silicon Technology"*, **(Invited)**, The 53rd Electronic Components and Technology Conference, May 27-30, (New Orleans, Louisiana) 2003

Fitzgerald, E.A., *"Heterogeneous Integration of SiGe, Ge and GaAs with Si"*, **(Invited)**, MRS Spring Meeting, April 21-25th (San Francisco, CA) 2003

P.N. Grillot and S.A. Ringel, "*Fermi level stabilization in plastically strained SiGe alloys,"* 45th TMS Electronic Materials Conference, June 23-27th (Salt Lake City, UT) 2003.

Y. Lin, O. Kwon, J. J. Boeckl, M.L. Lee, A. Pitera, E.A. Fitzgerald, and S.A. Ringel, "*Carrier recombination in metamorphic InAsP/InGaAs double heterostructure grown on off-cut and on-axis InP substrates,"* 45th TMS Electronic Materials Conference (Salt Lake City, UT) 2003.

S.A. Ringel, C.L.Andre, A.Khan, M. Gonzalez, M.K. Hudait, E.A.Fitzgerald, J.A. Carlin, M.T. Currie, C.W. Leitz and T.A.Langdo, "*Device-Quality III-V Compound Semiconductor Epitaxy on Si Via SiGe Interlayers*" (**Invited**), 49th American Vacuum Society International Symp. (Denver, CO), 2002.

Y. Lin, M.K. Hudait and S.A. Ringel, "*Growth of Compositionally-Graded InAsP and InAlAs Buffer Layers on InP Substrates Using Solid Source Molecular Beam Epitaxy*," 44th TMS Electronic Materials Conference (Santa Barbara, CA), 2002.

O. Kwon, C.L. Andre and S.A. Ringel, "*Growth and Properties of AlGaInP Laser Diodes Grown on GaAs and Ge Substrates by Solid Source Molecular Beam Epitaxy*," 44th TMS Electronic Materials Conference (Santa Barbara, CA), 2002.

C.L. Andre, A. Khan, M. Gonzalez, M.K. Hudait, E.A. Fitzgerald, J.A. Carlin, M.T. Currie, C.W. Leitz, T.A. Langdo, E.B. Clark, D.M. Wilt and S.A. Ringel, "Impact of Threading Dislocations on Both n/p and p/n Single Junction GaAs Cells Grown on Ge/SiGe/Si Substrates," Proc. 29th IEEE Photovolt. Spec. Conf. (New Orleans, LA), pp. 1043-1046, 2002.

M.K. Hudait, Y. Lin, C.L. Andre, P. Sinha and S.A. Ringel, "Relaxed InAsP Layers Grown on Step Graded InAsP Buffers by Solid Source MBE," Mater. Res. Soc. Symp. (San Francisco, CA) Proc. Vol. 719, pp. F13.3.1-F13.3.6, 2002.

S.A. Ringel**,** J.A.Carlin, C.L. Andre, J. Boeckl, C.W. Leitz, M. Currie, T. Langdo, E.A. Fitzgerald, A. Allerman, D.M. Wilt and E.B. Clark, "*Development of High Efficiency GaAs-on-Si Solar Cells Using GeSi Interlayers,*" Space Power Workshop (**Invited)**, Redondo Beach, CA, 2001.
O. Kwon and S. A. Ringel, "Growth and properties of lattice-matched and mismatched for mid-infrared devices grown on graded InAlAs/InP substrates InGaAs tunnel junctions," 43rd TMS Electronic Materials Conference, South Bend, IN, 2001.

S.A. Ringel, J.A. Carlin, C.L. Andre, M.K. Hudait, M. Gonzalez, D.M. Wilt, E.B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E.A. Fitzgerald and C.W. Leitz, "*Single junction InGaP/GaAs Solar Cells Grown on Si Substrates with SiGe Buffer Layers,"* (**Invited**) , Proc. 17th Space Photovoltaic Research and Technology Conf. (Cleveland), p. 160-177, 2001.

S.A. Ringel, J.A. Carlin, C.L. Andre and J. Boeckl, "*Development of High Efficiency GaAs-on-Si Solar Cells Using GeSi Interlayers,*" (**Invited**) NASA Solar Cell/Array Tech Review, Cleveland, OH, April 2001

S.A. Ringel, "*III-V Compound Photovoltaics on Si Using GeSi-Based Virtual Substrates,*" (**Invited**) Solar Energy Technology Review, Golden, CO, Oct. 2001.

2. Scientific Personnel Supported by this Program

Personnel receiving full or partial financial support:
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- **P.I.:** Professor Steven A. Ringel
- **Graduate Students and Staff:**
  Ojin Kwon, PhD Candidate
  Carrie Andre, PhD Candidate
  Matt Lueck, MS Candidate
  Dr. Mantu Hudait, Postdoctoral Researcher

MIT

- **P.I.**: Professor Eugene A. Fitzgerald
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  Gianni Taraschi

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Name	Degree/yr	position
Robert Sieg	PhD, 1999	Research Scientist, Sandia National Labs
John Carlin	MS, 1999; PhD, 2001	Research Engineer, Amberwave Systems
Carrie Andre	MS 2001; current PhD student	expected 4/04
Ojin Kwon	MS 2002; current PhD student	expected 4/05

Awards for ARO-supported students

Robert Sieg

- Best presentation, TMS Electronic Materials Conference 1998
- Ohio Space Grant Consortium Fellow

John Carlin

- NASA Graduate Student Researcher Program Fellow

Carrie Andre

- OSU University Fellow
- Ohio Space Grant Consortium Fellow
- OSU Presidential Fellow

MIT

Fully and partially ARO-supported students at MIT

Name	Degree/yr	position
Sanjeev Makan	MS, 1997	Fidelity Investments
Srikanth Samavedam	Ph.D., 1998	Motorola
Mayank Bulsara	Ph.D., 1998	Amberwave Systems Corp.
Steve Ting	Ph.D., 1999	TSMC
Andy Kim	Ph.D., 2000	Lumileds
Chris Leitz	Ph.D., 2002	Amberwave Systems Corp.
Vicky Yang	Ph.D., 2002	Amberwave Systems Corp.
Michael Groenert	Ph.D., 2002	Infineon
Gianni Taraschi	Ph.D., 2003	MIT Postdoc/ Dept. of Materials Sci. & Eng.
Lisa McGill	Ph.D., 2003	Intel, Portland, Oregon
Arthur Pitera	PhD anticipated	
Nava Ariel	PhD anticipated	
David Isaacson	PhD anticipated	

Awards for ARO-supported students

Advisor, Best Student Paper Award	TMS/IEEE Electronic Materials Conference (Sri Samavedam)	1997
Advisor, Best Student Presentation Award	TMS/IEEE Electrical Materials Conference (Andrew Kim)	1999
Advisor, Best Student Presentation Award	TMS/IEEE Electrical Materials Conference (Christopher Leitz)	2000
Advisor, Best Graduate Graduate Student Gold Award	MRS (Christopher Leitz)	2001
Advisor, Best Student Poster Award	MRS (Michael Groenert)	2001
Graduate Student Gold Award (Michael Groenert), Spring MRS		2002
Graduate Student Gold Award (Gianni Taraschi), Fall MRS		2002

Awards for Eugene Fitzgerald (past year)

Eugene Fitzgerald received a chaired professorship at MIT: The Merton C. Flemings – SMA

Professor of Materials Engineering (1/03-12/31/07)

3. Report of Inventions

U.S. Provisional Patent Application Ser. No. 60/406,882, "Improved Fabrication Method for Monocrystalline SiGe on Any Substrate", by Eugene A. Fitzgerald and Gianni Taraschi, MIT Case No. 9973

U.S. Patent Application Ser. No. 10/632,442 claiming priority to U.S. Provisional Patent Application Ser. No. 60/400,754 for "Yellow-Green Epitaxial Transparent Substrate-LEDS and Lasers Based on

Strained InGaP Quantum Well Grown on an Indirect Bandgap Substrate", by Eugene Fitzgerald and Lisa McGill, MIT Case No. 9944

Patent No. 6,805, 744, "Method of Producing Device Quality (AL) INGAP Alloys on Lattice-Mismatched Substrates", by Andy Kim and Eugene Fitzgerald, MIT Case No. 8288

International Patent Application Ser. No. PCT/US2005/042865, U.S Patent Application Ser. No. 10/999486, "Relaxed Ge and High-Ge Content Silicon-Germanium Alloy in Si with Low Dislocation Defects and Method for Making Same", by Eugene Fitzgerald and Minjoo Larry Lee, MIT Case No. 11326

International Patent Application Ser. No. PCT/US2005/035828, US Patent Application Ser. No. 10/956485, "Semiconductor Devices Having Bonded Interfaces and Methods for Making the Same", MIT Case No. 11368

International Patent Application Ser. No. PCT/US2005/035595, U.S Patent Application Ser. No. 10/956481, "Strained Gettering Layers for Semiconductor Processes", by David M. Isaacson, Eugene Fitzgerald, and Gianni Taraschi, MIT Case No. 11303

4. Scientific Progress and Accomplishment

This section reviews the scientific progress made under this contract since the last interim report (covers period 7/03-1/05). We review selected publications in this time period to highlight particular advances.

Strained SiGe Carrier Transport in MOSFETs

The ARO funding has supported basic work in relaxed SiGe and heterostructure grown thereon in the previous contract. In this contract period, we have largely finished this work, giving a heading to device engineers and industry which can lead to ever-more advanced versions of strained silicon germanium technology. In this period, we have been able to map mobility enhancements as a function of lattice constant, structure, and strain. This mapping has been published in Fitzgerald, E.A., M.L. Lee, C.W. Leitz and D.A. Antoniadis, "*MOSFET Channel Engineering Using Strained Si, SiGe, and Ge Channels*", **(Invited)**, 203rd Electrochemical Society Meeting, Spring, April 27-May 2nd 2003, Volume 2003-01, (Paris, France) 2003.

MOSFET CHANNEL ENGINEERING USING STRAINED SI, SIGE, AND GE CHANNELS

E.A. Fitzgerald,[1] M.L. Lee,[1] C.W. Leitz,[1] and D.A. Antoniadis[2]

[1]MIT, Department of Materials Science and Engineering, Cambridge, MA, 02139 USA
[2]MIT, Department of Electrical Engineering and Computer Science, Cambridge, MA 02139 USA

We have explored many MOSFET channel designs in the SiGe/Relaxed SiGe/Si system to explore the limits of electron and hole mobility in inversion layers. A versatile UHVCVD system and a long channel one-mask MOSFET process has allowed us to explore carrier mobility in hundreds of MOSFET inversion layer structures over the past five years. We show that the main challenge in enhancing MOSFET performance beyond conventional strained Si lies in understanding structures that enhance hole mobility at high inversion charge densities. The largest improvement in both PMOS and NMOS drive current enhancements were achieved with a ε-Si/ε-Ge/relaxed $Si_{0.5}Ge_{0.5}$ structure. At inversion charge densities of $\sim 10^{13}$ cm^{-2}, hole mobility and electron mobility were enhanced by 10x and 1.8x, respectively. The results in these MOSFETs show that the strained SiGe materials system possesses the potential to further reduce the power-delay product in CMOS far beyond conventional strained Si.

Lattice-Engineered Si-based Substrates

We had earlier realized that our progress in creating larger lattice constants such as SiGe on Si had created additional opportunities in inventing new engineered substrates, previously perceived to be impossible to create. The ability to engineer a different lattice on a substantially silicon substrate results in the ability to transfer large diameter thin layers of a different lattice to a handle silicon substrate (typically coated with an SiO_2 layer to aid in bonding).

The first demonstration of a wafer-scale engineered substrate (we had previously demonstrated the concept with pieces) was creating germanium on insulator (GOI) by transferring Ge onto a SiO_2/Si wafer from a Ge/$Si_{1-x}Ge_x$/Si lattice-engineered wafer. A strained SiGe layer was incorporated so that after layer exfoliation, the implant damage could be removed by etching to the embedded strained SiGe etch stop. This process has a great advantage as CMP or chemical etch methods to remove exfoliation implant damage results in a final GOI structure which has a large thickness variation in the top Ge layer.

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Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon by Wafer Bonding Ge/$Si_{1-x}Ge_x$/Si Virtual Substrates

Arthur J. Pitera,[z] G. Taraschi, M. L. Lee, C. W. Leitz,* Z.-Y. Cheng, and E. A. Fitzgerald

Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

We have demonstrated a general process which could be used for the integration of lattice-mismatched semiconductors onto large, Si-sized wafers by wafer bonding Ge/$Si_{1-x}Ge_x$/Si virtual substrates. The challenges for implementing this procedure for large diameter Ge-on-insulator (GOI) have been identified and solved, resulting in the transfer of epitaxial Ge/SiO_2 to a Si wafer. We found that planarization of Ge virtual substrates was a key limiting factor in the transfer process. To circumvent this problem, an oxide layer was first deposited on the Ge film before planarization using a standard oxide chemical mechanical planarization process. The GOI structure was created using H_2-induced layer exfoliation (Smartcut™) and a buried $Si_{0.4}Ge_{0.6}$ etch-stop layer, which was used to subsequently remove the surface damage with a hydrogen peroxide selective etch. After selective etching, the crosshatched surface morphology of the original virtual substrate was preserved with roughness of <15 nm rms as measured on a 25 × 25 μm scale and a 1 × 1 μm scale roughness of <1.4 nm. Using an etch-stop layer, the transferred device layer thickness is defined epitaxially allowing for future fabrication of ultrathin GOI as well as III-V films directly on large-diameter Si wafers.
 [DOI: 10.1149/1.1757462]

Manuscript submitted July 14, 2003; revised manuscript received January 16, 2004. Available electronically May 19, 2004.

As in most innovative research, by combining wafer-bonding, lattice-engineering, and strained layer etch stops, we discovered new phenomenon that also lead to innovative structures. We noticed that the H implant, used in the exfoliation process, gettered H preferentially and changed the orientation of the H platlets that nucleate. This work led not only to a better understanding of the exfoliation process and the interaction of implanted ions with strained layers, but it also suggested novel ways in which we can improve the exfoliation process.

JOURNAL OF APPLIED PHYSICS **97**, 104511 (2005)

Hydrogen gettering and strain-induced platelet nucleation in tensilely strained $Si_{0.4}Ge_{0.6}$/Ge for layer exfoliation applications

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(Received 2 February 2005; accepted 9 March 2005; published online 10 May 2005)

We show that tensilely strained epitaxial layers getter interstitially dissolved hydrogen and accelerate the nucleation of platelets. Both of these result in subsurface crack propagation leading to surface blistering and eventual exfoliation of a H^+-implanted semiconductor surface. In this work, a strained $Si_{0.4}Ge_{0.6}$ layer was used to enhance the exfoliation kinetics of relaxed Ge/$Si_{1-x}Ge_x$/Si virtual substrates by gettering hydrogen and providing a preferential nucleation site for platelets. Using platelet morphology and strain relaxation data, a nucleation and growth model was formulated accounting for both chemical and strain energy contributions to the free energy of platelet formation, revealing two kinetically limited growth regimes for platelets in tensilely strained $Si_{0.4}Ge_{0.6}$ films. Low-temperature (<200 °C) annealing nucleates 10^{11}-cm^{-2} platelets which grow in the strain-limited regime with minimal loss of hydrogen to surface effusion. At 250 °C, platelet growth is diffusion limited, requiring transport of H_2 molecules to the strained layer. Subsequent annealing of strained $Si_{0.4}Ge_{0.6}$/Ge gettering structures at a temperature exceeding 300 °C results in significantly improved surface blistering kinetics over samples which do not contain a gettering layer. Incorporation of tensilely strained layers has the potential of reducing the implantation dose and annealing temperature necessary for layer transfer. Combined with virtual substrate bonding, they provide a promising solution for economical integration of high-performance semiconductors with silicon. [DOI: 10.1063/1.1900928]

After understanding the materials science and physics behind the interaction between H implants and tensile strained SiGe layers embedded in the metamorphic Ge layer on Si, we were able to optimally design a double-strained-layer system in which one strained layer was used to enhance the exfoliation process and the other strained layer was used to act as an etch-stop layer. This structure was shown to be an ideal system for creating uniform GOI with a reduced dose (or lower temperature) for the exfoliation process. The reduced dose option lowers the cost of the overall process, whereas the lower temperature helps open up the window for transfer of temperature sensitive layers, or to more temperature sensitive substrates. These results are captured in the ECS2004 proceedings:

HYDROGEN GETTERING STRUCTURES FOR IMPROVED GERMANIUM LAYER EXFOLIATION PROCESSES

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Abstract. A novel Ge layer transfer structure employing the dual functionality of strained $Si_{0.4}Ge_{0.6}$/Ge layers is presented. First, the etch-stopping behavior of $Si_{0.4}Ge_{0.6}$ was used to fabricate thin Ge-on-insulator (GOI) by transferring these layers from relaxed $Si_{1-x}Ge_x$ graded buffers. Secondly, the H-gettering behavior of $Si_{0.4}Ge_{0.6}$/Ge is shown to reduce the thermal budget of Ge layer exfoliation processes. Recent data also indicates that strained SiGe layers also getter the point defects that are generated during the H implantation process and may also be useful for reducing the dose required for layer exfoliation. Incorporation of both an etch-stop and H-gettering layer with a virtual substrate bonding scheme will allow integration of thin mismatched layers on large diameter Si substrates while reducing thermal processing.

Ending our summary of our work in the Lattice-Engineered Substrates is our work on creating strained silicon on silicon (SSOS). By transferring a strained silicon layer directly to another silicon wafer (without oxide in between) we were able to demonstrate the first homochemical heterojunction, in which the strain-state of the material defines the band offsets of the heterostructure. These results were also presented at the ECS2004 meeting and published in the proceedings:

STRAINED SILICON ON SILICON BY WAFER BONDING AND LAYER TRANSFER FROM RELAXED SIGE BUFFER

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Thomas A. Langdo
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Abstract. We report the creation of strained silicon on silicon (SSOS) substrate technology. The method uses a relaxed SiGe buffer as a template for inducing tensile strain in a Si layer, which is then bonded to another Si handle wafer. The original Si wafer and the relaxed SiGe buffer are subsequently removed, thereby transferring a strained-Si layer directly to Si substrate without intermediate SiGe or oxide layers. Complete removal of Ge from the structure was confirmed by cross-sectional transmission electron microscopy as well as secondary ion mass spectrometry. A plan-view transmission electron microscopy study of the strained-Si/Si interface reveals that the lattice-mismatch between the layers is accommodated by an orthogonal array of edge dislocations. This misfit dislocation array, which forms upon bonding, is geometrically necessary and has an average spacing of approximately 40nm, in excellent agreement with established dislocation theory. To our knowledge, this is the first study of a chemically homogeneous, yet lattice-mismatched, interface.

III-V/Si Integration: Materials

The ARO program has previously led to the development of high quality III-V materials deposited on silicon substrates using SiGe interlayers. This promising work has led to impressive device demonstrations (see a later section) but also has spurred more materials investigations, resulting in further advancement.

One of the questions that has arisen is that, even though we have achieved high quality material with near-equilibrium lattice constants of III-V materials at room temperature, there will still be a critical thickness for cracking due to the difference in thermal expansion coefficient between III-V materials and the silicon substrate. We investigated the critical thickness for cracking in III-V layers on silicon, with and without SiGe interlayers. This information is critical for the design of integrated, planar III-V/Si devices.

Crack formation in GaAs heteroepitaxial films on Si and SiGe virtual substrates

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(Received 25 October 2002; accepted 14 January 2003)

We have determined the critical cracking thickness, or the thickness beyond which crack formation is favored, in GaAs films grown on Si and SiGe virtual substrates analytically and experimentally. The analytical model predicts a critical cracking thickness proportional to the biaxial modulus and the crack resistance of the GaAs film, and inversely proportional to the square of the thermal stress and a nondimensional crack resistance number Z. This Z number is determined by the mechanical properties of the GaAs film for a system without substrate damage, and is also determined by the mechanical properties of the substrate for a system with substrate damage. The experimentally determined critical thicknesses were in general greater than the analytically derived values due to the kinetic barriers to crack nucleation, which were not taken into consideration in the models. In addition, we have observed an asymmetric crack array formation, where arrays running in the ⟨110⟩ substrate off-cut direction are favored. We have also performed finite element modeling of the crack systems to study the evolution of thermal stress around crack planes in the GaAs film. [DOI: 10.1063/1.1558963]

In addition to understanding the formation of cracks, we also wanted to determine the impact of misfit and threading dislocation density on the luminescence efficiency of InGaAs quantum wells grown on metamorphic Ge/SiGe/Si. To this end, we deposited control InGaAs quantum wells on Si, GaAs, Ge, and Ge/SiGe/Si substrates and compared the materials with structural characterization techniques as well as with quantitative cathodoluminescence. An interesting result is that the quantum wells on Ge/SiGe/Si emit more luminescence than the control Ge substrate, and close to the amount of luminescence on GaAs control samples.

Comparison of luminescent efficiency of InGaAs quantum well structure grown on Si, GaAs, Ge, and SiGe virtual substrate

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(Received 4 December 2002; accepted 31 January 2003)

In order to study the luminescent efficiency of InGaAs quantum wells on Si via SiGe interlayers, identical $In_{0.2}Ga_{0.8}As$ quantum well structures with GaAs and $Al_{0.25}Ga_{0.75}As$ cladding layers were grown on several substrates by an atmospheric metalorganic vapor deposition system. The substrates used include GaAs, Si, Ge, and SiGe virtual substrates. The SiGe virtual substrates were graded from Si substrates to 100% Ge content. Because of the small lattice mismatch between GaAs and Ge (0.07%), high-quality GaAs-based thin films with threading dislocation densities $<3\times10^6\ cm^{-2}$ were realized on these SiGe substrates. Quantitative cathodoluminescence was used to compare the luminescent efficiency of the quantum well structure on the different substrates and cross-sectional transmission electron microscopy was used to characterize dislocation densities. Our results show that the InGaAs quantum wells grown on the GaAs substrates have the highest luminescent efficiencies due to the lowest dislocation densities. Interestingly, InGaAs quantum wells grown on the SiGe virtual substrates outperform those on Ge substrates, both in terms of luminescent efficiency and dislocation density. This difference is attributed to the variation in thermal expansion coefficient (α) and its impact on defect structure during the process cycle. The SiGe virtual substrate has a smaller α compared to a Ge substrate because of the smaller α of the Si substrate, which helps minimize compressive strain in the quantum well layer during the temperature decrease from the growth temperature. Consequently, fewer misfit dislocations are created between the quantum well and cladding interfaces. These misfits can greatly affect the luminescent efficiency since they can act as recombination sites. In general, the efficiencies of the quantum wells on the SiGe and Ge substrates were affected only by higher misfit dislocation densities, whereas the quantum wells on the Si substrate had low efficiency due to high threading dislocation density. [DOI: 10.1063/1.1563031]

Finally, we also performed a set of experiments to elucidate the effect of threading dislocation density on solar cell III-V structures on top of Ge/SiGe/Si substrates. It was discovered that n+/p and p+/n structures behave very differently. This can be understood by the fact that the minority carrier diffusion length of electrons is much larger than the minority carrier diffusion length of holes in III-V material. Thus, for III-V solar cells integrated on silicon, which will possess some residual threading dislocation density, p+/n junctions will out-perform n+/p junctions. A model was developed to further understanding of recombination in these structures.

Impact of dislocation densities on n^+/p and p^+/n junction GaAs diodes and solar cells on SiGe virtual substrates

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(Received 1 September 2004; accepted 11 April 2005; published online 7 July 2005)

Recent experimental measurements have shown that in GaAs with elevated threading dislocation densities (TDDs) the electron lifetime is much lower than the hole lifetime [C. L. Andre, J. J. Boeckl, D. M. Wilt, A. J. Pitera, M. L. Lee, E. A. Fitzgerald, B. M. Keyes, and S. A. Ringel, Appl. Phys. Lett. **84**, 3884 (2004)]. This lower electron lifetime suggests an increase in depletion region recombination and thus in the reverse saturation current (J_0 for an n^+/p diode compared with a p^+/n diode at a given TDD. To confirm this, GaAs diodes of both polarities were grown on compositionally graded $Ge/Si_{1-x}Ge_x/Si$ (SiGe) substrates with a TDD of 1×10^6 cm^{-2}. It is shown that the ratio of measured J_0 values is consistent with the inverse ratio of the expected lifetimes. Using a TDD-dependent lifetime in solar cell current–voltage models we found that the V_{oc}, for a given short-circuit current, also exhibits a poorer TDD tolerance for GaAs n^+/p solar cells compared with GaAs p^+/n solar cells. Experimentally, the open-circuit voltage (V_{oc}) for the n^+/p GaAs solar cell grown on a SiGe substrate with a TDD of $\sim1\times10^6$ cm^{-2} was ~880 mV which was significantly lower than the ~980 mV measured for a p^+/n GaAs solar cell grown on SiGe at the same TDD and was consistent with the solar cell modeling results reported in this paper. We conclude that p^+/n polarity GaAs junctions demonstrate superior dislocation tolerance than n^+/p configured GaAs junctions, which is important for optimization of lattice-mismatched III–V devices. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1946194]

Metamorphic III-V Integration

We have continued our efforts to generalize the metamorphic engineering we have gained in the SiGe/Si materials system to III-V materials systems. One of the systems we have continued to explore under the ARO contract is the InGaP/GaP materials system. This materials systems offers a way to reach direct band gaps that span from the red to the green. However, relaxed InGaP metamorphic graded layers tend to show the appearance of phase-separated regions (that can lead to defective regions) which we have explored in InGaAs and InGaP systems. We have further studied these defects in metamorphic InGaP. We have proven that these regions are likely to be caused by In concentration differences between regions.

Microstructural defects in metalorganic vapor phase epitaxy of relaxed, graded InGaP: Branch defect origins and engineering

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(Received 22 April 2004; accepted 1 June 2004; published 27 July 2004)

Strain-relaxed, compositionally graded InGaP layers grown by atmospheric-pressure metalorganic vapor phase epitaxy (APMOVPE) have previously been found to exhibit unusual contrast in transmission electron microscopy (TEM). The features that generate this contrast were termed "branch defects." Branch defects have been shown to pin threading dislocations and are thus undesirable features for the realization of low dislocation density semiconductors. In this study, we compare the properties of branch defects formed during optimized, relaxed, graded InGaP buffer deposition in two different reactor configurations: a commercial, multiwafer, low-pressure reactor and a custom-built, atmospheric-pressure research reactor. Branch defect formation is further characterized via the introduction of *in situ* annealing interruptions during graded buffer deposition in the atmospheric-pressure system. Branch defects are observed in material from both reactor systems, suggesting that they are a phenomenon intrinsic to InGaP graded buffer growth. Careful TEM studies of the resulting samples reveal that the phase space for the formation of branch defects is similar in both reactor configurations. During standard optimized graded buffer growth, higher growth temperatures delay the onset of branch defect formation to higher indium fractions in the graded buffer. Low growth temperatures produce branch defects at lower indium fractions, and these defects tend to be more closely spaced. In addition, the formation of branch defects is favored by low V/III ratios and *in situ* growth interruption and annealing. Annealing is found to create anisotropic strain relaxation in the graded buffer, which we attribute to the blocking of gliding threading dislocations by preferentially oriented branch defects. Based on the observed properties of branch defects and the factors that affect their formation, it appears that these defects are a manifestation of local variations in indium concentration that develop on the sample surface during MOVPE and are buried in the bulk due to kinetic limitations.
[DOI: 10.1116/1.1775003]

Device Demonstrations

As we have always stretched to do under the ARO grant (and by leveraging other funding), we perform device demonstrations incorporating our materials advances. This philosophy proves that we are truly making process in creating new materials and structures that are useful, but also lead to revealing important areas for further materials research. Publications that transmit such device demonstrations published in this period are:

Monolithic integration of room-temperature cw GaAs/AlGaAs lasers on Si substrates via relaxed graded GeSi buffer layers

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Harry Lee and Rajeev J. Ram
Department of Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts 02139

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(Received 21 June 2002; accepted 9 October 2002)

$GaAs/Al_xGa_{(1-x)}As$ quantum well lasers have been demonstrated via organometallic chemical vapor deposition on relaxed graded $Ge/Ge_xSi_{(1-x)}$ virtual substrates on Si. A number of GaAs/Ge/Si integration issues including Ge autodoping behavior in GaAs, reduced critical thickness due to thermal expansion mismatch, and complications with mirror facet cleaving have been overcome. Despite unoptimized laser structures with high series resistance and large threshold current densities, surface threading dislocation densities for GaAs/AlGaAs lasers on Si substrates as low as 2×10^6 cm^{-2} permitted continuous room-temperature lasing at a wavelength of 858 nm. The laser structures are uncoated edge-emitting broad-area devices with differential quantum efficiencies of 0.24 and threshold current densities of 577 A/cm^2. Identical devices grown on commercial GaAs substrates showed similar behavior. This comparative data agrees with previous measurements of near-bulk minority carrier lifetimes in GaAs grown on Ge/GeSi/Si substrates. [DOI: 10.1063/1.1525865]

Improved room-temperature continuous wave GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers fabricated on Si substrates via relaxed graded Ge_xSi_{1-x} buffer layers

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(Received 3 July 2002; accepted 31 March 2003; published 6 May 2003)

Improved GaAs/AlGaAs quantum well lasers were fabricated with longer lifetimes, higher efficiencies, and lower threshold current densities than previously reported devices on Ge/GeSi relaxed graded buffers on Si substrates. Uncoated broad-area lasers operated continuously at 858 nm with a differential quantum efficiency of 0.40 and a threshold current density of 269 A/cm^2. Similar devices fabricated on GaAs substrates demonstrated nearly identical performance. Operating lifetimes on Si substrates were nearly 4 h, a 1 order of magnitude improvement over previous devices. In addition, strained InGaAs quantum well lasers have been operated continuously at room temperature on Ge/GeSi/Si substrates with a differential quantum efficiency of 0.26 and a threshold current density of 700 A/cm^2. Electroluminescence analyses of the failure behavior of both types of devices have suggested that recombination-enhanced defect reactions are limiting laser lifetime on Si substrates. [DOI: 10.1116/1.1576397]

Yellow-green emission for ETS-LEDs and lasers based on a strained–InGaP quantum well heterostructure grown on a transparent, compositionally graded AlInGaP buffer

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Department of Materials Science and Engineering
Massachusetts Institute of Technology
Cambridge, MA 02139, U.S.A.

ABSTRACT

Epitaxial-transparent-substrate light emitting diodes with a primary emission peak at 590nm and a secondary peak at 560nm have been fabricated in the indium aluminum gallium phosphide (InAlGaP) system. The active layer consists of an undoped, compressively strained indium gallium phosphide (InGaP) quantum well on a transparent $In_{0.22}(Al_{0.2}Ga_{0.8})_{0.78}P$/ $\nabla_x[In_x(Al_{0.2}Ga_{0.8})_{1-x}P]$/GaP virtual substrate. Theoretical modeling of this structure predicts an accessible wavelength range of approximately 540nm to 590nm (green to amber). Emission with a peak wavelength of 570nm has been observed via cathodoluminescence studies of undoped structures with a quantum well composition of $In_{0.35}Ga_{0.65}P$. Light emitting diodes have been fabricated utilizing simple top and bottom contacts. The highest LED power of 0.18μW per facet at 20mA was observed for a quantum well composition of $In_{0.32}Ga_{0.68}P$ and a bulk threading dislocation density on the order of $7x10^6$ cm^{-2}. The spectrum of this device was composed of two peaks: a weak peak at the predicted 560nm wavelength and a stronger peak at 590nm. Based upon superspots present in electron diffraction from the quantum well region, we believe that the observed spectrum is the result of emission from ordered and disordered domains in the active region. The same device structure grown with a bulk threading dislocation density on the order of $5x10^7$ cm^{-2} exhibited an identical spectral shape with a reduced power of 0.08μW per facet at 20mA. For a quantum well composition of $In_{0.37}Ga_{0.63}P$ and an overall threading dislocation density on the order of $5x10^7$ cm^{-2}, a single peak wavelength of 588nm with a power of 0.06μW per facet at 20mA was observed.

Growth and properties of AlGaInP resonant cavity light emitting diodes on Ge/SiGe/Si substrates

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(Received 21 July 2004; accepted 26 October 2004; published online 11 January 2005)

Visible AlGaInP resonant cavity light emitting diodes (RCLEDs) were grown by molecular beam epitaxy and fabricated on low-dislocation density, SiGe/Si metamorphic substrates. A comparison with identical devices grown on GaAs and Ge substrates shows that not only did the RCLED device structure successfully transfer to the SiGe/Si substrate, but also a higher optical output power was obtained. This result is attributed to enhanced lateral current spreading by the low residual dislocation density ($\sim 1 \times 10^6$ cm^{-2}) network within the virtual Ge substrate and the superior thermal conductivity of the underlying Si wafer. In addition, the growth of an AlGaAs current spreading layer and a modified top metal contact were incorporated in the RCLED on SiGe to optimize device performance. The measured electroluminescent output power was 166 μW at a 665 nm peak wavelength under 500 mA current injection. Extremely narrow electroluminescence linewidths were achieved with a full width half maximum value of 3.63 nm under 50 mA current injection. These results demonstrate great promise for the monolithic integration of visible band optical sources with Si-based electronic circuitry.
[DOI: 10.1063/1.1835539]

Electrochemically controlled transport of lithium through ultrathin SiO_2

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Monolithically integrating the energy supply unit on a silicon integrated circuit (IC) requires the development of a thin-film solid-state battery compatible with silicon IC fabrication methods, materials, and performance. We have envisioned materials that can be processed in a silicon fabrication environment, thus bringing local stored energy to silicon ICs. By incorporating the material directly onto the silicon wafer, the economic parallelism that silicon complementary metal-oxide-semiconductor (CMOS) technology has enjoyed can be brought to power incorporation in each IC on a processed wafer. It is natural to look first towards silicon CMOS materials, and ask which materials need enhancement, which need replacement, and which can be used "as is." In this study, we begin by using two existing CMOS materials and one unconventional material for the construction of a source of electric power. We have explored the use of thermally grown silicon dioxide (SiO_2) as thin as 9 nm acting as an electrolyte material candidate in a solid-state power cell integrated on silicon. Other components of the thin-film cell consisted of rf-sputtered lithium cobalt oxide ($LiCoO_2$) as the cathode and highly doped *n*-type polycrystalline silicon (polysilicon) grown by low-pressure chemical-vapor deposition as the anode. All structures were fabricated using conventional microelectronics fabrication technology. The charge and discharge behaviors of the $LiCoO_2/SiO_2$/polysilicon cells were studied. On the basis of the impedance measurements an equivalent circuit model of an ultrathin cell was inferred, and its microstructure was characterized by electron microscopy imaging. In spite of its high series resistance ($\sim 4 \times 10^7\ \Omega$), we have shown that an ultrathin layer of an as-deposited Li-free SiO_2 is an interesting candidate for an electrolyte or controllable barrier layer in lithium-ion-based devices. © *2005 American Institute of Physics*.
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5. Technology Transfer

Bridging the university-commercialization gap is always a difficult process. We have previously been successful at commercializing ARO basic research concepts. For example, we formed AmberWave Systems Corporation and it has successfully transferred strained silicon technology to the marketplace. This process also created intellectual interest in this process, and we consider commercialization of other ARO concepts to be of high priority.

To this end, two ventures have been created to help commercialize our research output. Prof. Fitzgerald and Prof. Ringel have formed 4Power LLC, a company that will explore commercializing high efficiency solar cell technology on silicon, fabricated in a silicon fabrication environment. Additionally, Prof. Fitzgerald has formed Paradigm Research LLC, an organization meant to facilitate technology transfer to other organizations besides start-up enterprises.